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(54) IMPROVEMENTS IN ATTENUATOR CIRCUITS

(71) We, G. & E. BRADLEY LIMITED, a British company, of Electrical House, Neasden Lane, London, N.W.10., do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

This invention relates to attenuator circuits.

According to the present invention there is provided an attenuator circuit including a pair of input terminals and a pair of output terminals, first, second and third impedance arrangements, and a pair of diodes oppositely poled with respect to and connected in parallel with one another, the first impedance arrangement being connected between one of the input terminals and one of the output terminals, the second impedance arrangement being connected between the output terminals, the said diodes and the third impedance arrangement being connected in series with one another between the output terminals, and each of the said impedance arrangements consisting of a parallel combination of a capacitor and a resistor.

A fourth impedance arrangement may be connected between the other input terminal to the other output terminal.

The said pair of diodes conduct only when more than ½ volt is applied thereto if the diodes are germanium diodes and 1 volt if they are silicon diodes. Other magnitudes can be obtained by using d.c. bias, or by using zener diodes, for example.

The invention will now be described by way of example with reference to the drawings accompanying the Provisional Specification in which:

Figure 1 is a circuit diagram of an embodiment of the invention, and

Figure 2 is a diagram illustrating the operation of the embodiment of Figure 1.

In Figure 1 there is shown an attenuator circuit 10 having a pair of input terminals 11 and 12 and a pair of output terminals 13 and 14, one 12, of the input terminals being connected directly to one, 14, of the output terminals and the other input terminal 11 being connected to the other output terminal 12 through a parallel combination of a capacitor 15 and a resistor 16. The output terminals 13 and 14 are interconnected through another parallel combination of a capacitor 17 and a resistor 18 and through an arrangement consisting of a pair of diodes 19 and 20 connected in parallel with and reversely poled relative to one another, and a further parallel combination of a capacitor and a resistor, the diodes being in series with the capacitor 21 and resistor 22.

In use the diodes 19 and 20 do not conduct provided input signals applied across the input terminals 11 and 12 do not exceed a certain amplitude determined by the nature of the diodes. When this amplitude is exceeded, one or the other of the diodes conducts depending upon the polarity of the input signal. If the input signal is an alternating signal, the diodes conduct alternately.

When the diodes are not conducting, the attenuator circuit effectively consists of the capacitors 15 and 17 and resistors 16 and 18 only. To ensure that the attenuation effected thereby does not vary with frequency it is arranged that the relationship

$$\frac{C_1}{C_2} = \frac{R_2}{R_1}$$

is satisfied where C_1 and C_2 are the values of the capacitances of the capacitors 15 and 17 respectively and R_1 and R_2 are the values of the resistances of the resistors 16 and 18 respectively.

When either of the diodes is conducting the capacitor 21 and the resistor 22 are added and greater attenuation is effected. To ensure that the attenuation effected in this case does not vary with frequency it is also arranged that the relationship

$$\frac{C_1}{C_2 + C_3} = \frac{R^1}{R_1}$$

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is satisfied where R^1 is the value of resistance presented by the parallel combination of the resistors 18 and 22 and C_3 is the value of the capacitance of the capacitor 21.

In Figure 2 the continuous line 23 illustrates the output voltage obtained from the output terminal 13 of the attenuator circuit of Figure 1 when sinusoidal input voltage having an amplitude greater than the said certain amplitude is applied across the input terminals 11 and 12. During a first time interval T1 the input voltage at the input terminal 11 rises from the negative voltage level above which the diode 20 does not conduct to the positive voltage level below which the diode 19 does not conduct. Consequently the portion of the output voltage obtained during the time interval T_1 is the result of attenuation of the input voltage by the resistors 16 and 18 and the capacitors 15 and 17 only. During a second time interval T_2 the input voltage is above the said positive voltage level so that the diode 19 conducts and the capacitor 21 and resistor 22 are included in the effective attenuator. A broken line 24 in Figure 2 shows what the output voltage form would be if the diode 19 did not conduct. During a third time interval T_3 the input voltage falls from the said positive voltage level to the said negative voltage level, the diodes 19 and 20 do not conduct, and the portion of the output voltage obtained during this interval is the result of attenuation by the resistors 16 and 18 and the capacitors 15 and 17 only. The input voltage is below the said negative level during a fourth time interval T_4, the diode 20 therefore conducting and the capacitor 21 and the resistor 22 being again included in the effective attenuator. The form of the output voltage which would be obtained if the diode 20 did not conduct is shown by a broken line 25 in Figure 2. Operation during a fifth time interval T_5 is exactly the same as in the first time interval T_1.

It will be seen from Figure 2 that the output voltage which would be obtained if the diodes 19 and 20 did not conduct would be sinusoidal. Hence it will be realised that when the amplitude of a sinusoidal input voltage applied to the attenuator does not exceed the said certain value, the output voltage obtained is a sinusoid which is an attenuated version of the input voltage. Similarly for other forms of input voltage which do not cause the diodes to conduct the output voltage has the same shape as the input voltage.

The form of the output voltage obtained when the input voltage does cause one or both of the diodes to conduct at some times during the application of the input voltage to the attenuator is a composite of the output voltage obtained when the attenuation effected is due to the capacitors 15 and 17 and the resistors 16 and 18 only and that obtained when all the capacitors 15, 17 and 21 and resistors 16, 18 and 22 are effective. The positive and negative output voltage levels at which the change in attenuation takes place is indicated by a pair of broken horizontal lines 26 and 27 respectively in Figure 2.

When a push-pull input arrangement is required, the embodiment of Figure 1 can be modified by including a fourth parallel combination of a capacitor and a resistor between the input terminal 12 and that end of the resistor 22 which is connected to the output terminal 14 and removing the earth connection shown in Figure 1. The capacitor and resistor of the fourth parallel combination should be identical to the capacitor 15 and resistor 16 respectively.

The diodes 19 and 20 may be replaced by zener diodes.

The embodiment described is particularly useful as an attenuator in the triggering circuit of the time base of a cathode ray oscilloscope which is required to display voltages having widely varying amplitudes since a high gain trigger amplifier for amplifying small voltages up to a level sufficient to trigger the time base can be employed after the attenuator without the inconvenience of having to switch out the amplifier when larger input voltages are applied, the attenuator being designed to introduce the capacitor 21 and resistor 22 when sufficiently larger input voltages appear. Also the attenuator provides some protection against cramping and overloading of the amplifier by unexpectedly large input signals.

WHAT WE CLAIM IS:—

1. An attenuator circuit including a pair of input terminals and a pair of output terminals, first, second and third impedance arrangements, and a pair of diodes oppositely poled with respect to and connected in parallel with one another, the first impedance arrangement being connected between one of the input terminals and one of the output terminals, the second impedance arrangement being connected between the output terminals, the said diodes and the third impedance arrangement being connected in series with one another between the output terminals, and each of the said impedance arrangements consisting of a parallel combination of a capacitor and a resistor.

2. An attenuator circuit according to claim 1, wherein a fourth impedance arrangement is connected between the other input terminal to the other output terminal.

3. An attenuator circuit according to claim 1 or 2, wherein the said diodes are zener diodes.

4. An attenuator circuit substantially as described hereinbefore with reference to the drawings accompanying the Provisional Specification.

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PROVISIONAL SPECIFICATION

This drawing is a reproduction of the Original on a reduced scale.

FIG. 1.

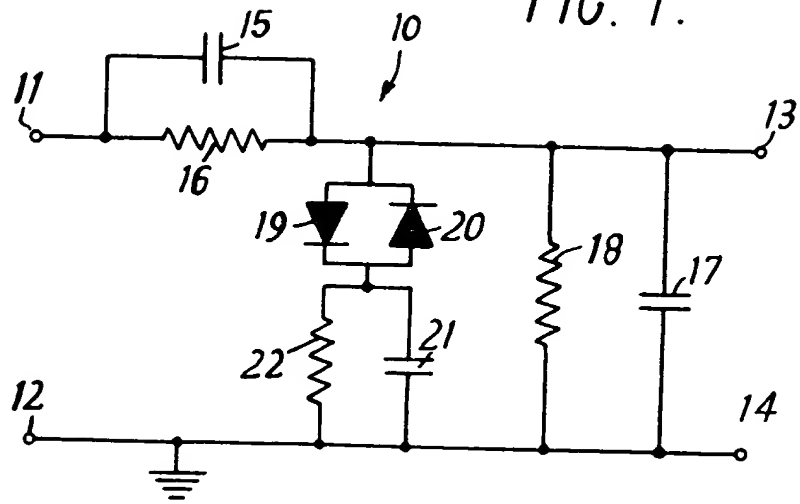
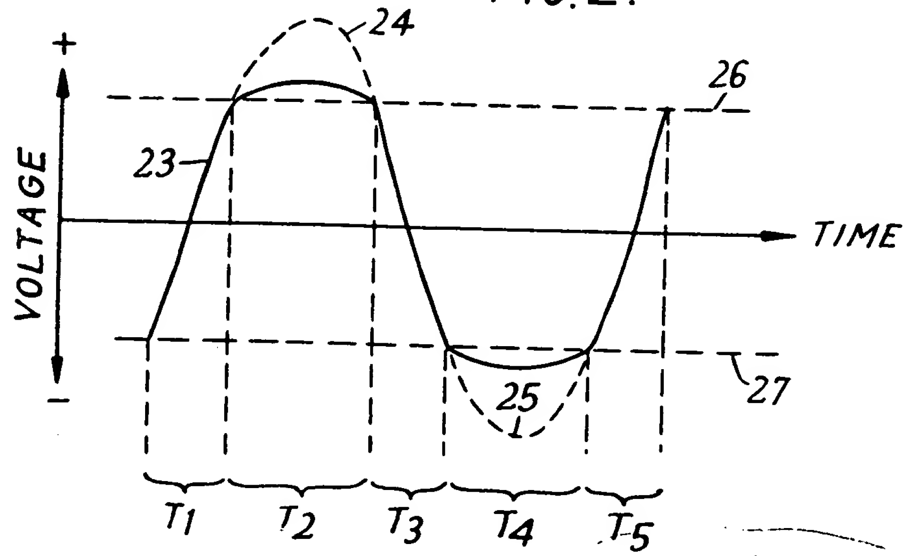


FIG. 2.



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